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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,470	03/09/2000	Hiroshi Katakura	000267	3147

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/522,470	KATAKURA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *8 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 06/14/2006.

2. Claims 1, 8, and 18 are pending in this application. Claims 1, 8, and 18 are independent claims. In Amendment, claims 2-7 and 9-17 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeman (U.S. 4,870,302).

Re claim 8, Freeman discloses in Figure 2 a logic circuit comprising: a first inversion section (e.g. 21) for inverting a first input signal (e.g. A) a first logic level and outputting an inverted first input signal (e.g. bar(A)); a second inversion section (e.g. 22) for inverting a second input signal (e.g. B) having a logic level always being opposite to the first logic level (e.g. A and B are two variables which can be opposite each other as one is complementary of other), and outputting the inverted signal (e.g. bar(B)); and a transmission section (e.g. transmission lines that connect all signals to 23-26) for receiving the inverted first input signal and the inverted second input signal and

outputting one of the inverted first input signal (e.g. output controls by C2 and bar(C2)) and the inverted second input signal (e.g. output controls by C3 and bar(C3)), a first switching section (e.g. area including transmission lines of A, bar(A) and C2, bar(C2)) provided on an input side of first inversion section and performing switching of whether the first input signal is passed to the first inversion section or blocked in accordance with an external control signal (e.g. phase 1, phase 2, or pass device in Figure 5); and a second switching section (e.g. area including transmission lines of B, bar(B) and C3, bar(C3)) provided on an input side of second inversion section and performing switching of whether the second input signal is passed to the second inversion section or blocked in accordance with the external control signal (e.g. phase 1, phase 2, or pass device in Figure 5), wherein the transmission section comprises electrically (e.g. must have current applied in order these logic gates operate in Figure 2) connected transistors (e.g. these OR, AND, XNOR... in Figure 2 must have at least one transistor or in another words, these logic gates are composed of multiple transistors) that respectively receive the inverted first input signal and the inverted second input signal, and the connected transistors output one of the inverted first input signal and the inverted second input signal in response to only an externally controllable selection signal (e.g. Cs and col. 2 lines 1-19) and an inverted signal of the selection signal (e.g. bar(Cs)).

Re claim 18, it has same limitations cited in claim 8. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Allowable Subject Matter

5. Claim 7 is allowed.

Response to Arguments

6. Applicant's arguments filed 06/14/2006 have been fully considered but they are not persuasive.

a. The applicant argues in page 6 third paragraph for claims 8 and 18 that the support for the feature of the first and second switching section provided on input sides of the first and second inversion sections respectively is found in Figure 20 and description in application specification on page 76 line 23 to page 77 line 17.

The examiner respectfully submits that Figure 20 and specification page 76 line 23 to page 77 line 17 do not quite provide the support for the claim features cited above. In the claims, they require only one external control signal for controlling both the inputs of the inversion sections whereas Figure 20 and specification discloses multiple external control signals (e.g. the external control signal as I and its complement signal as XI in Figure 2). In addition, the complement input signal XA is always input into the inverter regardless of the state of external control signal I or XI because the complement input signal XA is fed directly into the inverter 5c.

b. The applicant argues in pages 7-8 for claim 8 that the cited reference fails to disclose the first and second switching section provided at input side of first and second inversion sections respectively for turning on or off signal into the inversion sections.

The examiner respectfully submits that the on or off switching sections are also taught in Figure 5 of the invention as dynamic configuration logic (e.g. phase 1, phase 2, or pass device in Figure 5) for turning on or off the transmission of the input signal into the next component of logic circuit as clearly seen in Figure 5.

c. The applicant argues in page 8 last paragraph for claim 8 that the cited reference by Freeman fails to disclose the selection is done in response to only an externally controllable selection signal and its inverted signal.

The examiner respectfully submits that the number of externally controllable selection signal and its inverted signal is depending on the number of input signals. As seen in Figure 2, it requires more than two controlled signals because they are used to select more than two input signal. In Figure 3B, it requires 4 external control signal and 4 its inverted control signal for controlling or selecting 16 input signals. Basically, it requires 2xN external controllable signals for controlling 2^N input signals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,450,022 to New discloses a structure and method for configuration of a field programmable gate array.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 4, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100